external terminals electrically connected to the interconnect pattern; and

a plurality of insulating layers formed around the external terminals on the interconnect pattern, the insulating layers including an upper layer and a lower layer of different characteristics, the upper and lower layers made of resin.--

B5 cont.

REMARKS

Claims 1-36 are pending. Claims 25-36 have been previously withdrawn from consideration.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

Reconsideration based on the following remarks is respectfully requested.

I. The Specification Satisfies All Formal Requirements

The Office Action asserts that a statement reading "This application is a continuation of PCT application number PCT/JP00/01387 filed on March 8, 2000" should be included on page 1, line 1 of the specification." This assertion is respectfully traversed.

The present application is not a continuation of the PCT application, but is instead a 371 of the PCT application. Thus, such a statement is not required in the specification.

II. The Claims Satisfy All Formal Requirements

The Office Action objects to claims 21-24 as being of improper dependent form. This objection is respectfully traversed.

Claim 21 further limits claim 1 because it recites "a circuit board", while claim 1 does not recite this feature. Claim 22 further limits claim 13 because it recites "a circuit board", while claim 13 does not recite this feature. Claim 23 further limits claim 1 because it recites "an electronic instrument", while claim 1 does not recite this feature. Claim 24 further limits

claim 13 because it recites "an electronic instrument", while claim 13 does not recite this feature.

Withdrawal of the objection to the claims is respectfully requested.

III. The Claims Define Patentable Subject Matter

The Office Action rejects claims 1, 3-6, 8-10, 13, 15-18, 21 and 22 under 35 U.S.C. §102(b) over Greer (U.S. Patent No. 5,470,787); claims 2, 7, 14, 23 and 24 under 35 U.S.C. §103(a) over Greer; claims 11, 12 and 19 under 35 U.S.C. §103(a) over Greer in view of Lehrer (U.S. Patent No. 4,972,251); and claim 20 under 35 U.S.C. §103(a) over Greer in view of Kitayama et al. (U.S. Patent No. 5,744,382). These rejections are respectfully traversed.

Regarding claims 1, 21, and 23, each of the external terminals is positioned in an opening portion formed in insulating layers. The opening portion has at least one step portion formed on its inside surface. Further, the insulating layers are made of resin. Such a structure allows for the stress in the external terminals to be effectively dispersed and absorbed. Greer does not disclose the insulating layers, forming an opening portion in which a step portion is formed, being made of resin.

Regarding claims 10, 13, 22, 24, 37 and 38, the upper and lower layers have different characteristics. Further, the upper and lower layers are made of resin. Thus, the stress in the external terminals are effectively dispersed and absorbed. As discussed above, Greer fails to disclose the upper and lower layers made of resin.

For at least these reasons, it is respectfully submitted that claims 1, 10, 13, 21, 22, 23, 24, 37 and 38 are patentable over the applied references. The dependent claims are likewise patentable over the applied references for at least the reasons discussed as well as for the additional features they recite. Applicants respectfully request that the rejections under 35 U.S.C. § 102 and §103 be withdrawn

IX. Conclusion

In view of the foregoing, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are earnestly solicited.

Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicants undersigned representative at the telephone number listed below.

Respectfully submitted,

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Date: November 29, 2002

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APPENDIX

IN THE CLAIMS:

1. (Amended) A semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes; ~~and~~

external terminals electrically connected to the interconnect pattern; and

~~wherein~~ a plurality of insulating layers ~~are~~ formed around the external terminals on the interconnect pattern, the insulating layers made of resin, the insulating layers respectively having holes formed therein to form an opening portion, each of the external terminals positioned in the opening portion, the opening portion having at least one step portion formed on its inside surface.

10. (Amended) ~~The~~ A semiconductor device ~~as defined in claim 1,~~ comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes;

external terminals electrically connected to the interconnect pattern; and

a plurality of insulating layers formed around the external terminals on the interconnect pattern, ~~wherein~~ the insulating layers ~~include~~ including an upper layer and a lower layer of different characteristics, the upper and lower layers made of resin.

13. (Amended) A semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes; and

external terminals electrically connected to the interconnect pattern;

wherein the interconnect pattern is formed on an insulating layer which ~~is formed of at least one layer~~ includes an upper layer and a lower layer of different characteristics and has protrusions and depressions, the upper and lower layers made of resin; and

wherein the external terminals are formed in the depressions.

21. (Twice Amended) A circuit board on which is mounted ~~the~~ a semiconductor device ~~as defined in claim 1~~ comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes;

external terminals electrically connected to the interconnect pattern; and

a plurality of insulating layers formed around the external terminals on the interconnect pattern, the insulating layers made of resin, the insulating layers respectively having holes formed therein to form an opening portion, each of the external terminals positioned in the opening portion, the opening portion having at least one step portion formed on its inside surface.

22. (Twice Amended) A circuit board on which is mounted ~~the~~ a semiconductor device ~~as defined in claim 13~~ comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes; and

external terminals electrically connected to the interconnect pattern,

wherein the interconnect pattern is formed on an insulating layer which includes an upper layer and a lower layer of different characteristics and has protrusions and depressions, the upper and lower layers made of resin; and

wherein the external terminals are formed in the depressions.

23. (Twice Amended) An electronic instrument having ~~the~~ a semiconductor device ~~as defined in claim 1~~ comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes;

external terminals electrically connected to the interconnect pattern; and

a plurality of insulating layers formed around the external terminals on the interconnect pattern, the insulating layers made of resin, the insulating layers respectively having holes formed therein to form an opening portion, each of the external terminals positioned in the opening portion, the opening portion having at least one step portion formed on its inside surface.

24. (Twice Amended) An electronic instrument having ~~the~~ a semiconductor device ~~as defined in claim 13~~ comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes; and

external terminals electrically connected to the interconnect pattern,

wherein the interconnect pattern is formed on an insulating layer which includes an upper layer and a lower layer of different characteristics and has protrusions and depressions, the upper and lower layers made of resin; and

wherein the external terminals are formed in the depressions.